NEW EXTRACTION METHOD FOR FET EXTRINSIC CAPACITANCES USING ACTIVE BIAS CONDITIONS

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ABSTRACT

A new procedure for extracting the extrinsic capacitances of FETs is presented. It requires measurements only in the active bias regime. The method utilizes the symmetry of the intrinsic FET in the forward and reverse biased operating regime. The extraction is performed analytically and does not require any optimization.

INTRODUCTION

FET linear and nonlinear modeling requires an unambiguous separation between bias independent extrinsic equivalent-circuit elements and the bias dependent intrinsic part. In common extraction procedures, the pinch-off bias state is used to determine the extrinsic elements ([1], [2]). In contrast to this, we apply active bias conditions for this purpose. The extraction at pinch-off has the following drawbacks, which are avoided by the new method.

1. The equivalent circuit in the “coldfet“ regime is ambiguous.
2. The extrinsic drain capacitance C_{pd} cannot be separated from the intrinsic one C_{ds}.
3. Due to measurement uncertainties the real parts of the extracted admittance parameters are often non-physical.
4. The extrinsic feedback capacitance is not included.
5. The extrinsic inductances must be known a priori to obtain reliable results.

With respect to all five issues, the new method yields better results. We demonstrate this by extracting data of a state-of-the-art GaAs MESFET from on–wafer S parameter measurements.

The basic idea is to utilize symmetry of the intrinsic FET in the forward and reverse-biased operating regime. In both regimes, a channel current flows and the depletion region under the gate has its normal extension. Except for the assumption of symmetric electrical behaviour under the gate metallization no further information on the intrinsic device is needed to extract the extrinsic capacitances. One should outline that this intrinsic symmetry relies on the channel characteristics under the gate and does not require a symmetrical layout of gate, drain, and source electrode (Fig. 1).

THE BASIC IDEA: SYMMETRIC FORWARD AND REVERSE BIAS POINT

The method starts from the standard FET equivalent circuit in Fig. 2 and the forward and reverse biased *I-V* characteristics (see Fig. 3). The two bias points

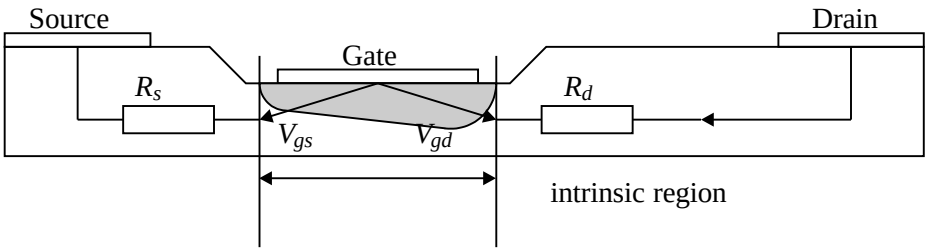

Fig. 1. Intrinsic region under the gate with symmetric electrical characteristic regarding forward and reverse biasing.

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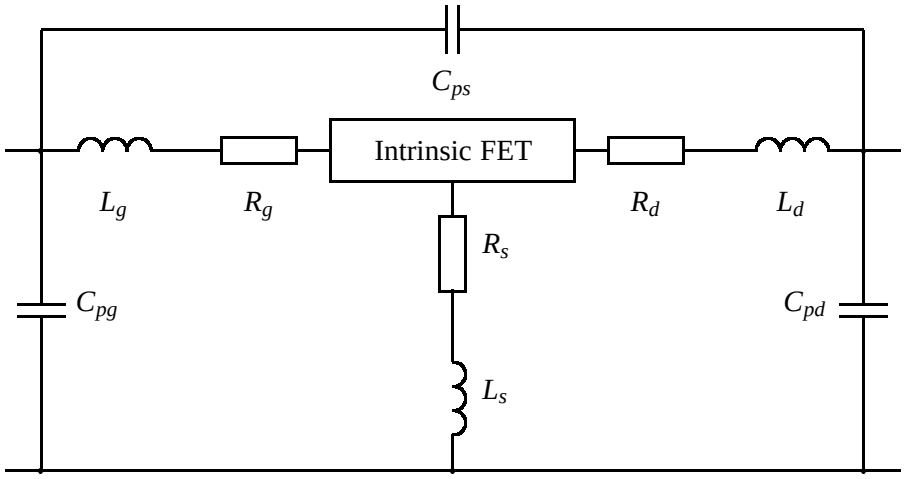

Fig. 2. FET equivalent circuit subdivided in intrinsic part and extrinsic network.

correspond to operating the intrinsic FET in common–source and common–drain configuration, respectively. With two external DC voltages V_{GSn} and V_{DSn} an unique operation point is set, which leads to the DC currents I_{gn} and I_{dn}. The intrinsic part of the FET only represents the section of the channel below the gate metal (Fig. 1). The internal DC voltages V_{gsn} and V_{dsn} differ from the external ones due to the voltage drop at the extrinsic resistances. In the symmetric reverse bias point, the space-charge region must have the same shape as in the normal bias point shown in Fig. 3. To arrive at this symmetric bias point, the following intrinsic bias conditions must be fulfilled:

$$V_{gdr} = V_{gsn} \quad \wedge \quad V_{dsr} = -V_{dsn} \tag{1}$$

In terms of current, the condition can be written as

$$I_{gr} = I_{gn} \quad \wedge \quad I_{dr} = -(I_{dn} + I_{gn}) \tag{2}$$

The gate current can be neglected since we are dealing with a depletion–type FET. Therefore, the drain current is the same in both cases, so that the voltage drop at the extrinsic resistance is identical, too. With this assumption, the symmetric reverse bias point can be adjusted with the external drain voltage $V_{DSr} = -V_{DSn}$ and the drain current $I_{dr} = -I_{dn}$. As a starting value for the voltages, first $V_{GSr} \approx V_{gsr} = V_{gdn} = V_{gsn} - V_{dsn}$ and, second, a negative drain voltage $V_{DSr} = -V_{DSn}$ is applied. Then, gate voltage is varied until the negative drain current $I_{dr} = -I_{dn}$ is reached. This variation in gate voltage is necessary because R_d and R_s are different.

EXTRACTION PROCEDURE

In order to obtain the extraction equations, one has to relate the measured quantities, i.e., the Y parameters of the complete circuit, to the intrinsic description at both bias points. This is accomplished in 3 steps:

1. The Z matrix of the intrinsic FET in the symmetric reverse bias point (Z_{ri}) is the common–source to common–drain transformation of the Z matrix (Z_{ni}) in the normal bias point:

$$\begin{aligned} Z_{ni} &= \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \\ Z_{ri} &= \begin{bmatrix} Z_{11}-Z_{12}-Z_{21}+Z_{22} & Z_{22}-Z_{12} \\ Z_{22}-Z_{21} & Z_{22} \end{bmatrix} \end{aligned} \tag{3}$$

2. In the next step the shell Z_{ext} containing the extrinsic resistances and inductances is added to Z_{ri} and Z_{ni}.

$$Z_{ext} = \begin{bmatrix} Z_g + Z_s & Z_s \\ Z_s & Z_d + Z_s \end{bmatrix} \tag{4}$$

$$\begin{aligned} Z_n &= Z_{ni} + Z_{ext} = \begin{bmatrix} Z_{n11} & Z_{n12} \\ Z_{n21} & Z_{n22} \end{bmatrix} \\ Z_r &= Z_{ri} + Z_{ext} = \begin{bmatrix} Z_{r11} & Z_{r12} \\ Z_{r21} & Z_{r22} \end{bmatrix} \end{aligned} \tag{5}$$

3. To obtain the Y parameters at the outer ports, which are the quantities measured, the extrinsic shell Y_{ext} must be added to both inverted matrices Z_r and Z_n.

$$Y_{ext} = \begin{bmatrix} Y_{pg} + Y_{ps} & -Y_{ps} \\ -Y_{ps} & Y_{pd} + Y_{ps} \end{bmatrix} \tag{6}$$

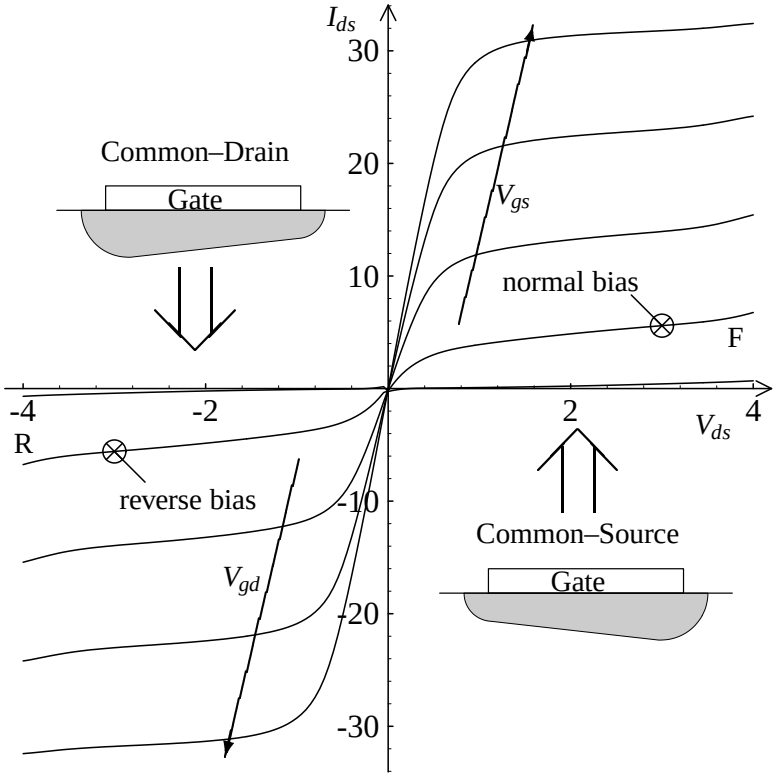

Fig. 3. I–V characteristics and the two symmetric bias points under normal and reverse conditions.

$$Y_{mn} = [Z_n]^{-1} + Y_{ext} = \begin{bmatrix} Y_{mn11} & Y_{mn12} \\ Y_{mn21} & Y_{mn22} \end{bmatrix}$$
$$Y_{mr} = [Z_r]^{-1} + Y_{ext} = \begin{bmatrix} Y_{mr11} & Y_{mr12} \\ Y_{mr21} & Y_{mr22} \end{bmatrix} \quad (7)$$

These two admittance matrices are known from the S parameter measurements in the forward and reverse bias point. With the identities for the Z parameters according to (3) equation (5) leads to

$$Z_{n12} - Z_{n21} = Z_{r21} - Z_{r12} \quad (8)$$
$$Z_{n11} - Z_{n12} = Z_{r11} - Z_{r21} \quad (9)$$
$$Z_{n22} = Z_{r22} \quad (10)$$

and a system of equations is derived that can be solved for Y_{pg}, Y_{ps}, and Y_{pd}:

$$|Y_{mr}| = Y_{mr11}Y_{mr22} - Y_{mr12}Y_{mr21}$$
$$|Y_{mn}| = Y_{mn11}Y_{mn22} - Y_{mn12}Y_{mn21}$$
$$a_1 = Y_{mn12}Y_{mr12}$$
$$a_2 = Y_{mn21}Y_{mr21}$$
$$a_3 = Y_{mn22}Y_{mr11}$$
$$a_4 = Y_{mn11}Y_{mr22}$$
$$a_5 = Y_{mn12} - Y_{mn21}$$
$$a_6 = Y_{mr12} - Y_{mr21}$$
$$b_1 = a_5 a_6 \left(|Y_{mn}| + |Y_{mr}| + a_1 + a_2 - a_3 - a_4\right)$$
$$Y_{ps} = \frac{a_2 - a_1 \pm \sqrt{b1}}{a_5 + a_6} \quad (11)$$
$$Y_{pg} = \frac{Y_{mr11}a_5 + a_6 Y_{mn11}}{a_5 + a_6} - Y_{ps} \quad (12)$$
$$Y_{pd} = \frac{Y_{mr22}a_5 + a_6 Y_{mn22} - a_2 + a_1}{a_5 + a_6} \quad (13)$$

The capacitances can be calculated from the imaginary parts of the Y parameters in equations (11)–(13).

$$C_{pg} = \frac{\mathrm{Im}\{Y_{pg}\}}{\omega} \quad C_{pd} = \frac{\mathrm{Im}\{Y_{pd}\}}{\omega}$$
$$C_{ps} = \frac{\mathrm{Im}\{Y_{ps}\}}{\omega} \quad (14)$$

The intrinsic FET parameters are only used to separate the influence of the extrinsic capacitances. In bias points with high drain currents, the intrinsic capacitance C_{gs} is much larger than the extrinsic ones, which

increases the influence of measurement errors. Therefore, the procedure should be applied at bias points with lower drain current.

In some special cases, the resulting FET equivalent circuit does not equal that of Fig. 2, e.g., if FET periphery is electrically large so that distributed networks have to be employed in describing the extrinsic elements. Then, the new method can be utilized to verify the extrinsic network extracted with the standard algorithm. By deembedding down to the intrinsic level, validity of equations (8)–(10) can be checked.

VALIDATION

As an example to validate the extraction routine we treat a $0.5 \times 80\,\mu\text{m}^2$ GaAs MESFET fabricated in-house. The FET is operated in active bias regime with $V_{DS} = 3\,\text{V}$. Extractions are performed at three different drain current values ($I_{ds} = \pm 5\,\text{mA}$, $\pm 10\,\text{mA}$, and $\pm 15\,\text{mA}$). Figs. 4–6 provide the extracted capacitance values. One observes good agreement between the three bias points, i.e., the capacitances are bias-independent as necessary. This verifies the new method and the underlying assumptions regarding symmetry.

CONCLUSIONS

FET extrinsic capacitances are determined from active bias two-port S parameter measurements in normal and reverse case. The calculation is straight forward and does not involve any optimization. The method can be employed without an a-priori-knowledge of the intrinsic device.

REFERENCES

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[2] M. White, R.M. Healy, "Improved Equivalent Circuit for Determination of MESFET and HEMT Parasitic Capacitances from "Coldfet" Measurement," *IEEE Microwave Guided Letters*, vol. 3, no. 12, pp. 453–454, December 1993.

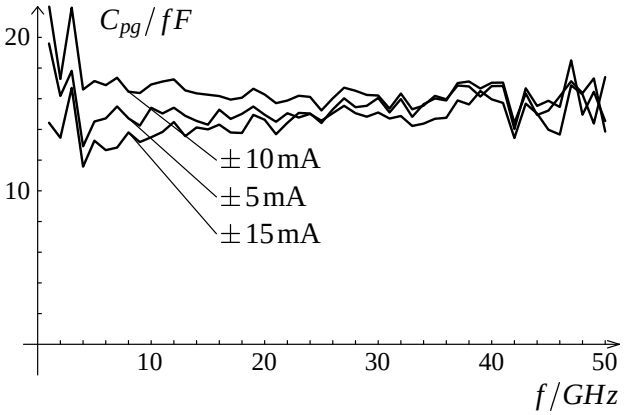

Fig. 4. Extracted value of extrinsic capacitance C_{pg} against frequency for $V_{ds} = 3\,\text{V}$ and three different drain currents $I_{ds} = \pm 5\,\text{mA}$, $\pm 10\,\text{mA}$ and $\pm 15\,\text{mA}$ ($0.5 \times 80\,\mu\text{m}^2$ GaAs MESFET).

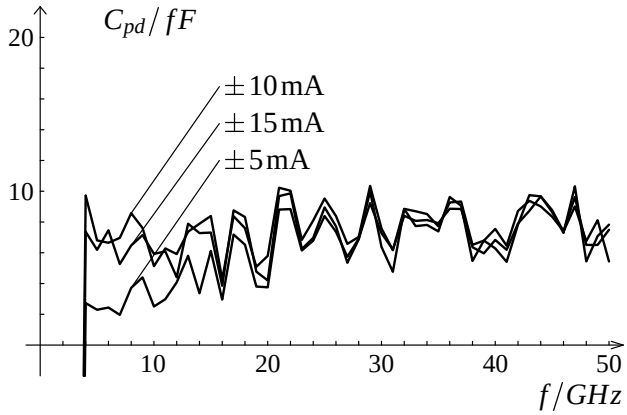

Fig. 5. Extracted value of extrinsic capacitance C_{pd} (all other data as in Fig. 4).

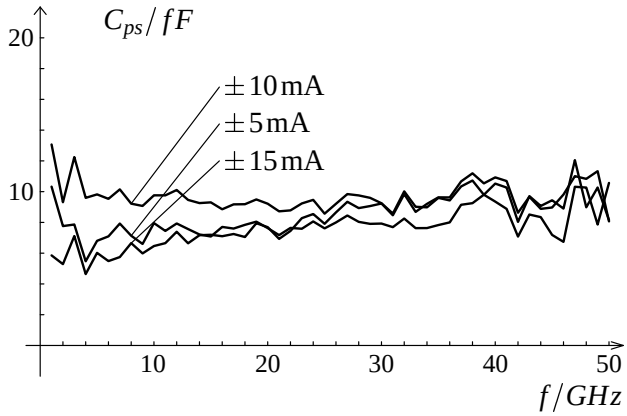

Fig. 6. Extracted value of extrinsic capacitance C_{ps} (all other data as in Fig. 4).